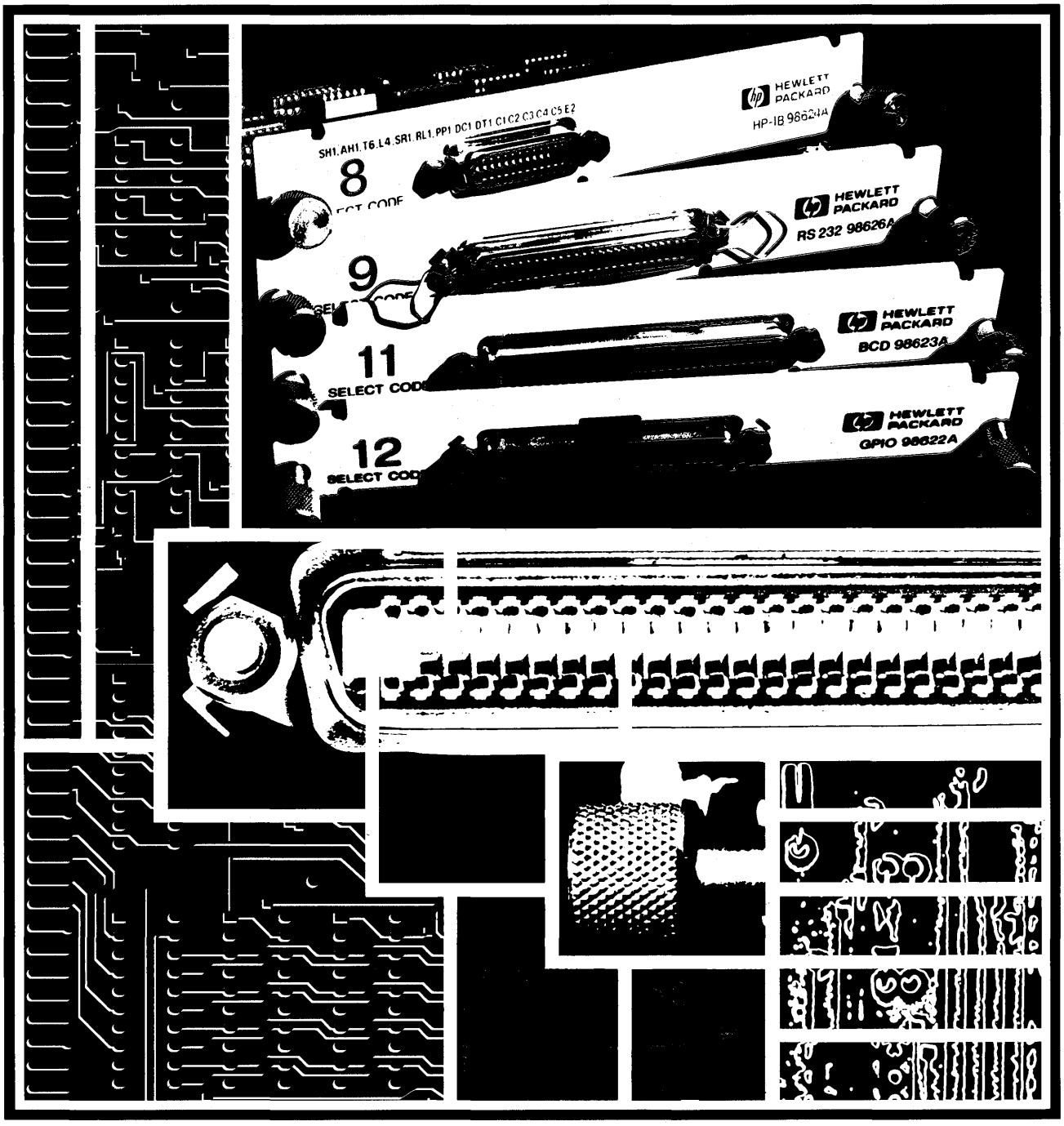
HP 98641A Option 001
Programmable Datacomm Interface
Remote Job Entry Using the CCITT V.35 Standard
(PDI RJE V.35)



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HP 9000 Series 300 Computer Systems

HP 98641A Option 001 Programmable Datacomm Interface Remote Job Entry Using the CCITT V.35 Standard (PDI RJE V.35)

Installation Manual

Card Assembly: 98641-66510
Date Code: A-2742

HEWLETT-PACKARD COMPANY
Roseville Networks Division
8000 Foothills Boulevard
Roseville, California 95678

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98641-90005

First Edition ..... November 1987

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Safety Considerations

General

This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

Safety Symbols

Instruction manual symbol: the product may be marked with this symbol. This refers the user to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal (sometimes used in the manuals to indicate circuit common connected to grounded chassis).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure or practice that, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure or practice that, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

Grounding

WARNING

SAFETY EARTH GROUND - The computer on which this product is installed is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the computer system is configured to match the available main power. Consult your system installation manuals.

Servicing

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by service-trained personnel.

Handling

CAUTION

STATIC SENSITIVE DEVICES

When any two materials make contact, their surfaces are crushed on the atomic level and electrons pass back and forth between the objects. On separation, one surface comes away with excess electrons (negatively charged) while the other is electron deficient (positively charged). The level of charge that is developed depends on the type of material. Insulators can easily build up charges in excess of 20,000 volts. A person working at a bench or walking across a floor can build up a charge of many thousands of volts. The amount of static voltage developed depends on the rate of generation of the charge and the capacitance of the body holding the charge. If the discharge happens to go through a semiconductor device and the transient current pulse is not effectively diverted by protection circuitry, the resulting current flow through the device can raise the temperature of internal junctions to their melting points. MOS structures are also susceptible to dielectric damage due to high fields.

The resulting damage can range from complete destruction to latent degradation. Small geometry semiconductor devices are especially susceptible to damage by static discharge.

THIS PRODUCT CONTAINS STATIC SENSITIVE DEVICES.

Transport or store printed circuit board assemblies in an antistatic container. When installing or removing the assemblies, do not touch any components. Hold each board by its edges. Component replacement operations must be performed at a static-free workstation using proper antistatic procedures.

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1

General Information

This manual provides general information, installation, theory of operation, programming information, maintenance instructions, replaceable parts information, and servicing diagrams for the HP 98641A Option 001 Programmable Datacomm Interface Remote Job Entry using the CCITT V.35 Standard (PDI RJE V.35).

This manual is divided into seven chapters as follows:

Chapter 1 - General Information

Chapter 2 - Installation

Chapter 3 - Theory of Operation

Chapter 4 - Maintenance

Chapter 5 - Replaceable Parts

Chapter 6 - Service Diagrams

Chapter 7 - Product History

General Description

The HP 98641A Option 001 PDI RJE V.35 is an interface card which allows an HP 9000 Series 300 to appear as a 2780 or 3780 Remote Job Entry Station to a remote computer mainframe. The features and functional interface of the PDI RJE V.35 gives the HP 9000 Series 300 batch file transfer capability to remote computers (especially IBM computers) over a CCITT V.35 direct connect data communication link.

The PDI RJE V.35 card uses several of the Z-80 family of microprocessor components to achieve significant off-loading of the HP 9000 Series 300 host computer. RJE link control functions, and numerous data preprocessing functions (e.g., character set conversion, blocking/deblocking, etc.) are performed automatically, releasing the host computer from much data communications overhead. Once configured, the PDI RJE V.35 card can provide record-at-a-time transfers of data to and from the HP 9000 Series 300 host computer.

Equipment Supplied

The HP 98641A Option 001 PDI RJE V.35 product consists of the following items:

a printed circuit assembly, part number 98641-66510;

a five-metre (16.4 feet) CCITT V.35 DTE (male) cable with test connector, part number 5062-3301;

a test hood, part number 5062-3302; and

an installation manual, part number 98641-90005.

Identification

The Product

Up to five digits and a letter (98641A in this case) are used to identify Hewlett-Packard products. The five digits identify the product; the letter indicates the revision level of the product. Options are identified by the word "Option," along with three digits (001 in this case).

Printed Circuit Assembly

The printed circuit assembly supplied with the HP 98641A Option 001 product is identified by a part number marked on the card. In addition to the part number, the assembly is further identified by a letter and a four-digit date code (e.g., A-2742). This designation is placed below the part number. The letter identifies the version of the etched circuit on the card. The date code (the four digits following the letter) identifies the electrical characteristics of the card with components mounted. Thus, the complete part number on the PDI RJE V.35 printed circuit assembly could be:

98641-66510
A-2742

NOTE

For brevity, the "printed circuit assembly" will be referred to merely as "card" in the remainder of this manual.

If the date code stamped on the card does not agree with the date code on the title page of this manual, there are differences between your card and the card described herein. These differences are described in manual supplements available at the nearest Hewlett-Packard Sales and Service Office (a list of Hewlett-Packard Sales and Service Offices is contained at the back of this manual).

Manual

This manual is identified by name and part number. The name, part number, and publication date are printed on the title page. If the manual is revised, the publication date is changed. The "Printing History" page records the reprint dates and manual update record.

Specifications

Table 1-1 lists the specifications of the HP 98641A Option 001 PDI RJE V.35 card.

Features

- Remote Job Entry (RJE) for batched-job communication with remote computers using IBM 2780/3780 bisync protocol.
- CCITT V.35 compatibility
- Supports externally provided baud rates of 1200, 1800, 2400, 3600, 4800, 7200, 9600, 19200, 38400, and 56000 baud
- Auto-answer and auto-turnaround capability
- 16K bytes of RAM, of which 3.5K bytes are used for data buffer storage
- Configurable parameters:

  Record/block sizes
  Timeouts
  Retry counts
  Character sets
  Conversion tables
  Record separators
  Formatting functions
  Variable or fixed length records

- Self-test contained in EPROM
- Support of EBCDIC line code
- Dial-up or private line communication, either half- or full-duplex
- Choice of transparent or nontransparent mode
- Choice of time-out or indefinite wait (if using dedicated leased lines)
- Link control functions:

  Line bid
  Normal and transparent data modes
  All responses (ACK/NAK/WACK/TTD/RVI)
  Link termination

- Special character handling:

  Character code translation
  Automatic record termination
  Adding/stripping record/block separator sequences
  Blank truncation/padding

- Long-term communication statistics to assist in line quality and link trouble shooting

Table 1-1. Specifications (Continued)

Physical Characteristics

Size (including mounting plate)	135 mm by 170 mm (5.3 by 6.6 inches)
Weight	310 grams (11 ounces)
Backplane Connector	100-pin edge connector
Device Connector	24-pin edge connector

Environmental Range

Operating	0 degrees C to +55 degrees C 5% to 95% relative humidity
Nonoperating	-40 degrees C to +75 degrees C

Power Requirements

Voltage	Current	Power Consumption
+5 Volts	0.710 Amperes	3.55 Watts
+12 Volts	0.037 Amperes	0.44 Watts
-12 Volts	0.060 Amperes	0.72 Watts

2

Installation

This chapter provides information on installing and checking the operation of the PDI RJE V.35 card.

Determining Current Requirements

The PDI RJE V.35 card obtains its operating voltages from the host computer. Before installing the card, it is necessary to determine whether the added current will overload the power supply. The current requirements of the card are listed in the power requirements entry of table 1-1. Refer to the appropriate system manual for the power supply capabilities.

Firmware (EPROM) Installation

CAUTION

Some of the components used in this product are susceptible to damage by static discharge. Refer to the safety considerations information at the front of this manual before handling the card or removing or replacing the components.

The EPROM (U29, see the parts location diagram in Chapter 6) is installed in a socket as shown on the parts location diagram. Ensure that the EPROM is installed properly, and that it has not been damaged or loosened from its socket during shipping.

Additionally, when installing or removing the EPROM, guard against bending or breaking the pins on the component. These pins also can be folded between the component and its socket, which would result in intermittent operation of the PDI RJE V.35 card. In most cases, a bent or damaged pin can be straightened with careful use of needlenose pliers.

Configuration Switches

Two eight-switch packs (SW1 and SW2) are located on the PDI RJE V.35 card as shown in figure 2-1. The left switch pack (SW2) is used to set the hardware interrupt level and the interface select code. The right switch pack (SW1) is not used by the PDI RJE V.35 card.

When setting the configuration switches, be sure the switch rockers are fully depressed and properly seated. Switch settings can be changed by using a ball-point pen or a similar pointed tool to depress each switch rocker.

Select Code Switches

Each interface must have a unique select code so that it can be accessed by the host computer. On the PDI RJE V.35 card, the select code is set by switches 0 through 4 on the left switch pack shown in figure 2-1. The settings and select codes are shown in table 2-2.

Select codes 0 through 7 should not be used. (Select codes 0 through 6 are reserved for internal peripheral devices such as the keyboard, disc drives, CRT display, etc.; select code 7 is used by the HP-IB interface.) Thus, select codes 8 through 31 are available for the PDI RJE V.35 card and other interfaces. The default select code setting for the PDI RJE V.35 is 20.

Interrupt Level Switches

Switches 5 and 6 on the left switch pack (SW2) determine the level on which the PDI RJE V.35 card will interrupt. Interrupt levels 1 and 2 are reserved for internal peripheral devices only, leaving interrupt levels 3 through 6 available for the PDI RJE V.35 card and other interfaces. Interrupt level 3 is lowest priority; 6 is highest priority. If an interrupt request conflict occurs, service is provided by the host computer on the basis of highest priority first.

The switch settings and the interrupt levels are shown below. The default interrupt level is 3.

Table 2-1. Interrupt Level Settings

Switch 6	Switch 5	Interrupt Level
0	0	3 (default)
0	1	4
1	0	5
1	1	6

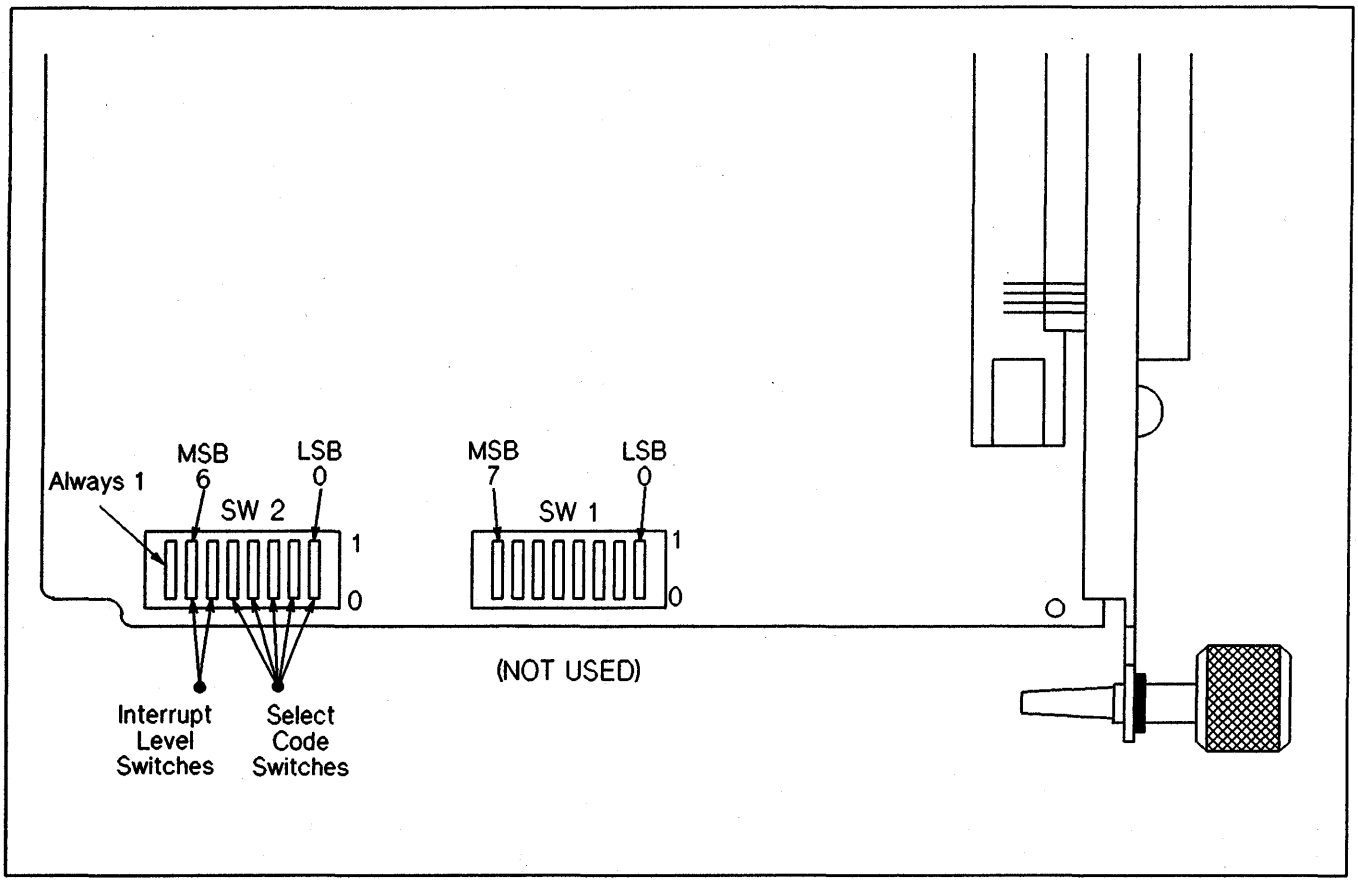


Figure 2-1. Configuration Switches

Table 2-2. Select Code Settings

MSB 4	3	2	1	LSB 0	Select Code
0	0	0	0	0	0 (Don't Use)
0	0	0	0	1	1 (Don't Use)
0	0	0	1	0	2 (Don't Use)
0	0	0	1	1	3 (Don't Use)
0	0	1	0	0	4 (Don't Use)
0	0	1	0	1	5 (Don't Use)
0	0	1	1	0	6 (Don't Use)
0	0	1	1	1	7 (Don't Use)
0	1	0	0	0	8
0	1	0	0	1	9
0	1	0	1	0	10
0	1	0	1	1	11
0	1	1	0	0	12
0	1	1	0	1	13
0	1	1	1	0	14
0	1	1	1	1	15
1	0	0	0	0	16
1	0	0	0	1	17
1	0	0	1	0	18
1	0	0	1	1	19
1	0	1	0	0	20
1	0	1	0	1	21
1	0	1	1	0	22
1	0	1	1	1	23
1	1	0	0	0	24
1	1	0	0	1	25
1	1	0	1	0	26
1	1	0	1	1	27
1	1	1	0	0	28
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31

Installation

CAUTION

Always ensure that the power of the computer is off before inserting or removing the PDI RJE V.35 card or cable. Failure to do so might result in damage to the PDI RJE V.35 card.

CAUTION

Some of the components used on the PDI RJE V.35 card are susceptible to damage by static discharge. Refer to the safety considerations information at the front of this manual before handling the card.

Install the PDI RJE V.35 card as follows:

1. Set the switches on the card for proper operation in your system. See figure 2-1 for the locations of the switches and the applicable paragraphs in this chapter for the switch settings.

2. Install the card in the appropriate I/O slot in the computer. Refer to the computer system installation manual for further information, if necessary. Components on the card must be on the same side as for other cards in the computer. When installing the card, use care not to damage components or traces on the card or on adjacent cards. Tighten the two thumbscrews (one on each side of the card) to seat the card firmly in place in the computer.

3. Connect the cable to the card.

Start Up

To start up and verify correct operation of the PDI RJE V.35 card, perform the following:

1. Turn on computer system power.

2. A self-test, which is executed at power on, is contained on the card. If the card does not pass self-test, a message will appear on the CRT indicating that the card has failed. If the PDI RJE V.35 card fails self-test, refer to Chapter 4 for maintenance instructions.

Reshipment

If the PDI RJE V.35 card is to be shipped to Hewlett-Packard for any reason, attach a tag identifying the owner and indicating the reason for shipment. Include the part number of the PDI RJE V.35 card.

Pack the card in the original factory packing material, if available. If the original material is not available, good commercial packing material should be used. Reliable commercial packing and shipping companies have the facilities and materials to repack the item. BE SURE TO OBSERVE ANTISTATIC PRECAUTIONS.

3

Theory of Operation

The HP 98641A Option 001 PDI RJE V.35 card allows an HP 9000 Series 300 computer to appear either as a 2780 or 3780 Remote Job Entry Station to a remote computer mainframe.

Functional Theory of Operation

A functional block diagram of the PDI RJE V.35 card is shown in figure 3-1. Reference should also be made, as necessary, to the schematic logic diagram, figure 6-1, in Chapter 6.

The PDI RJE V.35 card communicates with the mainframe through interface circuitry that is treated like memory addresses by the mainframe. Information is exchanged between the card and mainframe through shared RAM memory and hardware registers. Access to shared memory and hardware registers is obtained through the shared memory controller. Data is transferred on the shared data bus. Interface between the card and mainframe is managed by interrupt circuitry and the address comparator connected to the upper bits of the mainframe memory address bus.

The PDI RJE V.35 EPROM contains operating firmware for the Z-80 CPU (U28, see figure 6-1), which executes the programs stored in the EPROM. Shared memory is used to exchange information between the card Z-80 CPU and the mainframe. The Z-80 controls the Serial Input/Output (SIO) circuit (U27, see figure 6-1) and the Counter Timer Circuit (CTC, see U12 on figure 6-1). The SIO and CTC circuits perform serial I/O operation (SIO) and counter and timing functions (CTC). The Z-80 also performs and controls various other interface functions on command from the mainframe processor.

The Modem Control Register Latch (U6) and Modem Status Register Buffer (U5) hold control and status information being exchanged between a modem and the card. Line drivers (U1, U2, U3, U7, and U8) and receivers (U9 and U10) convert the internal TTL signals to CCITT V.35 electrical levels for transmissions over the datacomm link.

Z-80 Subsystem

The Z-80 CPU, SIO, and CTC circuits control the operation of the PDI RJE V.35 card. The CPU, SIO, CTC, and the ROM and default switches (SW1) are tied together through the internal Z-80 16-bit address bus (ZA) and 8-bit data bus (ZD). These buses belong exclusively to the PDI RJE V.35 card and are not accessible by the mainframe.

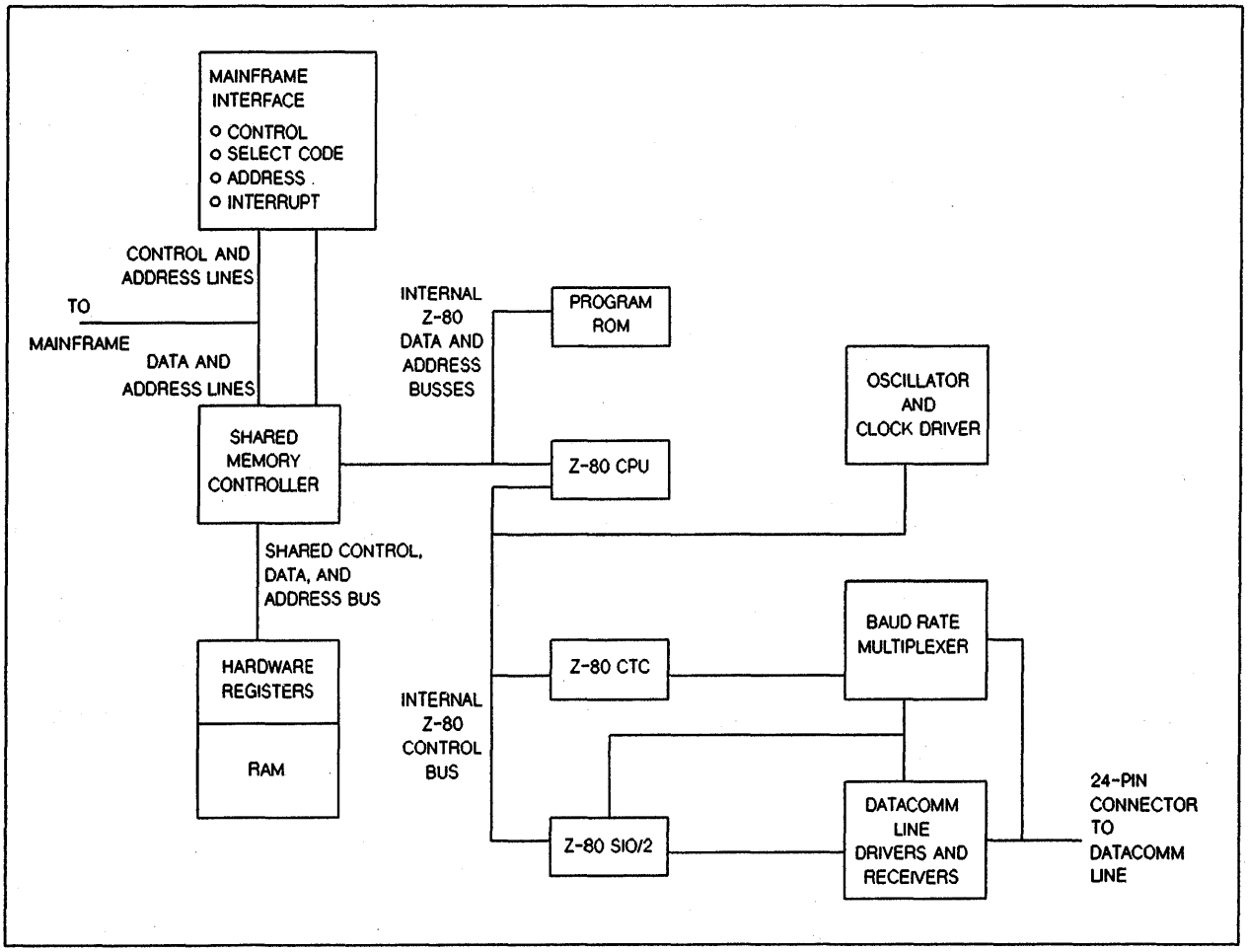


Figure 3-1. PDI RJE V.35 Functional Block Diagram

Shared RAM and registers are accessed through the shared data and shared address buses. Access to the shared buses is controlled by the Shared Memory Controller (see figure 3-1). In general, bus access is granted to the first processor that requests the bus. If the shared memory controller grants access to one processor and the other processor requests access during the memory cycle, the controller holds the second processor off until the memory cycle is complete, after which shared memory access is granted to the second processor. If a simultaneous-request conflict occurs, bus access defaults to the mainframe processor. Only 15 bits of address bus and 8 bits of data bus are gated to the shared buses from the mainframe. The remaining mainframe address bus bits are gated to the address comparator to establish select code identification. The address comparator bits combine with the shared address bus bits to establish the range of mainframe memory addresses that pertain to a particular device. Upper-byte mainframe data bus bits (8 through 15) are not used by the PDI RJE V.35 card.

Select Code Recognition

The Address Comparator (U43) decodes mainframe upper memory bits to detect card accesses. The BAS input from the mainframe gates the comparator inputs to ensure that the address is stable. When the address is recognized, the P=Q output is activated, causing the IMA (I'm Addressed) output to return acknowledgment to the mainframe. The DTACK (Data Acknowledge) output is also enabled, and is activated later by the Shared Memory Controller.

The signals BLDS (Buffered Lower Data Strobe) and MYPA (My Peripheral Address) are ANDed with the Request Enable flip- flop (U23, pin 4) to produce the mainframe shared memory request signal, one of the inputs to the Shared Memory Controller. The Request Enable flip-flop ensures that the Shared Memory Controller has completed any memory cycles in process before granting access for a new cycle, because the mainframe and card processors are not synchronized with each other.

Interrupt System

The mainframe driver enables or disables interface card interrupts by sending control sequences to the shared data bus that set or clear the Interrupt Enable flip-flop (U14, pin 5) through a hardware register access.

When the PDI RJE V.35 card determines that service from the mainframe is required, the interrupt condition is sent to a register in shared memory. The memory write cycle automatically resets the Interrupt Request flip-flop (U23, pins 9 and 10). If interrupts are enabled (Interrupt Enable Q output is low), and service is requested (Interrupt Request Q output is low), the Interrupt Demultiplexer (U34) is enabled. When the enable signal is received by the Interrupt Demultiplexer, the interrupt level switches are decoded (SW2, pins 6 and 7), which activates one of the interrupt request lines (IR3 through IR6).

Interrupt requests are cleared by the mainframe when it reads the Interrupt Condition register in shared memory. The interrupt request is removed when the Interrupt Register Decoder (U22) activates one of the Set inputs on the Interrupt Request flip-flop.

NOTE

A portion of RAM is shared by both the card and the mainframe. Some of these shared RAM locations are referred to as registers; the Interrupt Condition register is this type of register.

During power-up, the computer mainframe pulls the RESET input on all interface cards low. This causes the PDI RJE V.35 card to reset its Z-80 CPU by activating its reset input for the duration of the RESET pulse, and clears the Reset flip-flop (U15, pin 9). When the Reset flip-flop Q output goes low, it resets or presets other flip-flops that must be initialized to a known state. The Z-80 CPU then disables the Reset flip-flop during execution of its reset routines. A shared hardware register access is used to terminate the hardware reset.

When a control register operation is used to reset the card, the control sequence is handled through the Shared Memory Controller which sends the reset command to the Reset flip- flop. The flip-flop then:

- Disables mainframe interrupts by setting the Interrupt Enable flip-flop.
- Disables mainframe interrupt requests by setting the Interrupt Request flip-flop.
- Clears the hardware Semaphore flip-flop (semaphore busy).
- Initializes the CTC and SIO circuits by activating their Reset inputs.
- Disables Modem Control Latch (U6) outputs to ensure that the TR (Terminal Ready) and RS (Request-to-Send) lines are inactive until initialized by the Z-80 CPU.
- Initializes the baud rate Clock Dividers (U13) to ensure proper timing synchronization.
- Interrupts the Z-80 CPU through its Nonmaskable Interrupt (NMI) line. Note that during power-up when RESET is active, the RESET input is recognized by the Z-80, and the NMI input is ignored.

Shared Memory Controller

Addressing

Communication between the PDI RJE V.35 card and the mainframe is handled through a set of memory addresses, some of which are handled as registers. Only alternate addresses from the mainframe are used because the least significant bit is not connected (shared address bit 0 is connected to mainframe address bit 1, etc.). The upper two bits of the shared address bus (shared address bits 13 and 14, mainframe address bits 14 and 15) determine the data destination (write) or source (read) as follows:

Table 3-1. Address Bits

SA14	SA13	Source/Destination
0	0	Hardware Registers
0	1	RAM Lower Block (U25)
1	0	RAM Upper Block (U25)
1	1	Not Used

Shared memory addressing is accessed through a set of dual-input multiplexer/latch circuits (U39, U40, U41, U42). The Access Select flip-flop (U19, pin 9) selects the memory address from the mainframe or card CPU, then latches the address (U16, pin 3) to maintain proper signals during the memory cycle.

Read/Write Control

The mainframe read/write control line is buffered through the same multiplexer/latch circuits that handle memory addresses. U39, pin 15 carries mainframe read/write control (U39, pin 2) during mainframe memory accesses, and is held inactive during Z-80 accesses (U39, pin 3). The latched mainframe read/write signal controls the direction of the 8- bit bus transceiver (only the lower eight bits of the 16-bit bus are used), and drives the 2B (read/write) input of the memory control multiplexer.

The Z-80 read/write control line (ZRD) controls the direction of the shared data bus transceiver (U45), and drives the 2A (read/write) input of the memory control multiplexer (U32, pin 5). The Access Select flip-flop determines which input (2A or 2B) is used to drive the shared read (SRD) output which, when gated with shared memory timing clocks from U17, controls the RAM write enable (SWR) line.

Clock Circuits

The 7.3728 MHz oscillator drives a pair of flip-flop frequency dividers (U19, pins 1 through 6; and U15, pins 1 through 6) to generate symmetrical timing pulses at 1/2 and 1/4 the clock frequency, respectively. The 3.6864 MHz system clock output (TP5) is also used to drive the Z-80 clock input after being waveshaped by Q1, Q2, and their associated circuitry. The output of the second divider (U15, pin 6) produces a 1.8432 MHz frequency reference for the CTC circuit, which generates baud rate timing signals for the SIO circuit. CTC timing signals are fed to the SIO circuit through the baud rate multiplexer (U11).

Memory Access Select Timing

At the beginning of a processor memory cycle, the card or mainframe CPU sends a memory request. The Z-80 outputs A15, MREQ, and RFSH are combined (U24, pin 1) to drive the 1A input of the memory control multiplexer (U32). The mainframe BLDS output is combined with MYPA (TP6), then gated with shared memory timing (U17, pin 6 through U23 to U4, pin 11) to drive the 1B input of the memory control multiplexer (U32). The same line is also connected to the D input of the Access Control flip-flop, which selects the mainframe or card processor when its clock goes high.

The Access Control flip-flop is clocked when the oscillator and system clock (TP5) are both low (U24, pin 13 goes high). (Note that U16, pin 4 and U17, pin 6 are both low, indicating that no memory cycle is in progress.) The state of the Access Select flip-flop's D input at clock time determines which processor gets control of the shared memory cycle. If D is low, the mainframe processor is connected; if D is high, access defaults to the card's Z-80 processor. When the system clock (TP5) input to the timing chain goes high, the 1A or 1B input to the memory control multiplexer (U32) is selected by the Access Control flip-flop, inverted by the multiplexer, then used to start a memory cycle when the timing chain flip-flops (U17, pin 2) are clocked on the falling edge of the system clock (TP5).

Memory Cycle Timing

If no memory cycle is in progress, the shared memory access request lines from both processors are sampled on alternate falling edges of the 7.37 MHz clock when TP5 is low. If a memory cycle is in progress, request sampling is held off until the cycle is complete. The two memory cycle timing chain flip-flops (U17) control memory cycle timing.

A memory cycle timing diagram is shown in figure 3-2. The diagram shows the relationship of the clock oscillator (U18) and the system clock (TP5). Assume that all previous memory cycles have run to completion. The Shared Memory Controller samples the incoming memory request lines on alternate falling edges of the clock oscillator when the system clock at TP5 is low. When a shared memory access request is received, it propagates through intermediate gates and the memory control multiplexer (U32), then arrives asynchronously at the D input of the first timing chain flip-flop (U17, pin 2). If the request is from the mainframe, it arrives at the Access Select flip-flop's D input slightly earlier. (If a memory cycle is in progress, the access request from either processor is held off by U23, pins 3 and 14, which are held high by U17, pin 6. Both inputs go low at the end of the memory cycle, enabling any pending requests in order of established priority. The mainframe takes precedence in simultaneous pending requests.)

When TP5 is low, if a shared memory request is pending prior to the falling edge (B) of the clock oscillator, the Access Select flip-flop is clocked to determine which processor gets control of shared memory. The output of the flip-flop is then sent to the various multiplexers that control signal routing in the memory and hardware register circuitry.

After the multiplexers have had time to settle, the address latches (U39 through U42) are clocked on the next rising edge (C) of the clock oscillator (TP5 also goes high). The latched address then propagates to the RAMs and hardware register address decoding circuits.

On the next falling edge of the system clock (TP5), which is also the next rising edge of the clock oscillator (E), the shared memory request at the D input of the first timing chain flip-flop is clocked, causing the flip-flop to clear. The output change (Q output goes low) immediately disables clocking to the Access Select flip-flop and address multiplexer latches, and releases the Z-80 WAIT line if the Z-80 is selected. The 3Y or 4Y outputs of the memory control multiplexer (U32) are set to enable the appropriate data bus transceiver (U44 or U45), and the Shared Write (SWR) control line is gated to the RAM (U36, pins 4 and 5 both high). This sequence initiates a memory read or write cycle.

The memory access (read or write) is complete on the next falling edge (I) of the system clock (TP5). At this time, the second timing chain flip-flop is clocked, causing pin 8 to go low. This disables the SWR line, forcing it high (end of write cycle), and sends a DTACK (Data Acknowledge) to the mainframe if the mainframe has access to shared memory. The controller then hangs in the same state until the shared memory access request is removed by the processor. When the processor releases the request line, the D input (U17, pin 2) goes high, releasing the data bus transceivers. The timing chain then resets to its idle state. After the next rising edge to U17, pin 3, the controller is ready to process a new memory request.

Hardware Registers

The four read and four write registers that are implemented completely in hardware (RAM is not used) are selected when SA2 through SA14 are all 0 (U36, pin 8 low). The hardware register decoder (U21) combines SA0, SA1, and the shared read line to enable the appropriate register.

Only bit 7 is implemented in write registers 0 and 1. Register 0, interface reset, sets the Reset flip-flop (U15, pins 8 through 13). Register 1, interrupt enable, sets or clears the Interrupt Enable flip-flop (U14, pins 1 through 6).

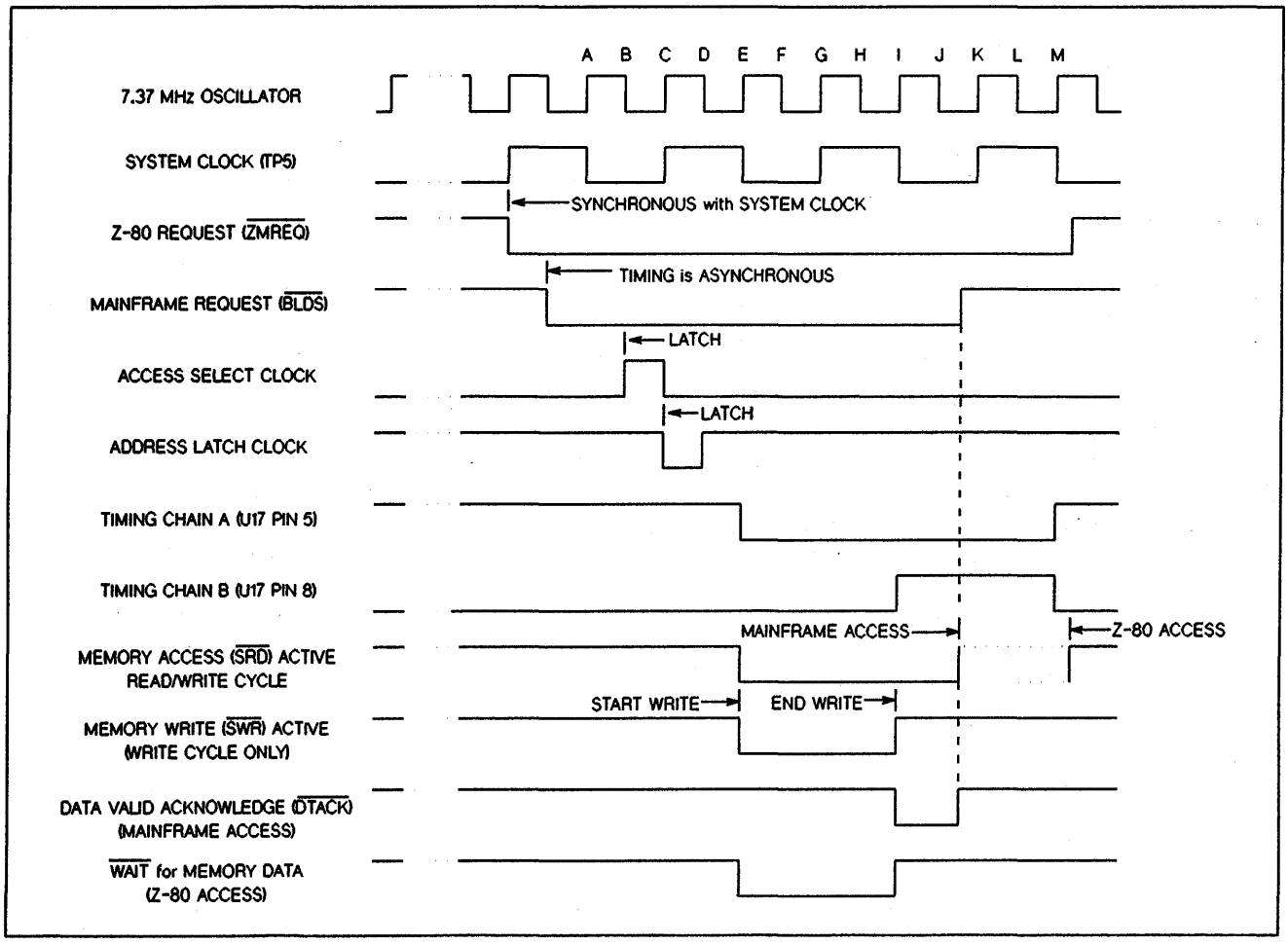


Figure 3-2. Memory Cycle Timing

The upper four bits (bits 4 through 7) of read registers 0 and 1 are implemented by the tri-state multiplexer (U33). SD0 through SD3 are held high (0) by pull-up resistors, except that SD2 is pulled low (1) by U33, pin 3 during reads from register 0 (interface ID). Read register 0 provides the Switch R setting (SW2, pin 8) and card identification to the shared data bus. Read register 1 provides the interrupt level switch settings, state of the interrupt request flip- flop, and the state of the interrupt enable flip-flop.

Register 3 is the modem control and status register. Data written to this register is latched by the modem control latch (U6). Data inputs are taken from the modem status register buffer (U5).

Register 2 controls the hardware semaphore. Data inputs (read register) sample the state of the semaphore flip-flop (U14, pin 8). At the end of the read access, the flip-flop is clocked, causing the output to be set (D input is always 1). A write to this register clears the flip-flop by pulsing the clear line. The semaphore is normally used as a hold-off flag to tell the other processor that a resource is in use and is not available until the current operation has been completed. At the end of the operation, the semaphore is cleared to enable access by the other processor. This provides a means to protect the integrity of shared data without risk of scrambling buffer and queue pointers and data.

Shared RAM

RAM address space is divided into two segments: lower and upper blocks. The first two locations of the lower block are also connected to special decoding hardware that control interrupts between the processors that share the memory. One register is used as a Command register; the other as an Interrupt Condition register. When commands are sent from the mainframe to the card Command register, the command flip-flop is set, causing an interrupt to the card processor through the SIO CTSB input. Data placed in the Interrupt Condition register by the card processor sets the Interrupt Request flip-flop, which then interrupts the mainframe processor if interrupts are enabled.

4

Maintenance

If the PDI RJE V.35 card did not pass the self-test described in Chapter 2, it is recommended that you return the card to Hewlett-Packard. If further testing is desired, however, a test hood can be used to test more of the card's circuitry. The test hood, part number 5062-3302, is included with the product.

The PDI RJE V.35 card self-test is programmed in ROM and functionally tests portions of the hardware on the card. (If a test hood is installed, more hardware is tested.)

The self-test includes a ROM test, a RAM test, a CTC test, an SIO test, a semaphore test, and a frontplane loopback test. There are two ways to invoke self-test: it is automatically invoked during power up when the Auto Reset line is pulled low, or it may be invoked dynamically by a Self-test interrupt from the host computer.

CAUTION

The host must *NOT* attempt to interrupt the PDI RJE V.35 card until it has received a Self-test Done interrupt from the card.

Test Hood

As noted above, a test hood is included with the product. The test hood (part number 5062-3302) connects to connector J1. When the test hood is installed, a pattern is generated in a section of the self-test that externally loops back through the line drivers and receivers.

Self-test results are interpreted by user interface software. If the test hood is installed and the user interface software indicates that the self-test is OK, the card passed the self-test. If the card did not pass self-test, the software will print the select code of the card and identify it either as a 98628 card or a 98641 card. This indicates that the card failed self-test.

To test the card using the test hood, perform the following:

1. Turn computer system power off.
2. Connect the test hood (part number 5061-3302) to connector J1.
3. Turn on computer system power. The self-test will execute.

Upon successful completion of self-test, the following will occur:

1. The card will send the host a Self-test Complete interrupt.
2. A message will be displayed on the system console identifying the card as a 98641V at 20. This indicates that the card passed self-test.
3. The card will execute the initialization routine.

Upon unsuccessful termination of self-test, the following will occur:

1. All registers are pushed onto the stack.
2. The system console will display the card's select code, will identify the card as either a 98628 or 98641, and will specify it failed.
3. The card sends the host a Self-test Complete interrupt.
4. The Z-80 is halted. Interrupts are disabled at this point.

Repair

If desired, isolation to a defective part may be performed. Please be advised, however, that such work is at your discretion and is your responsibility; moreover, NOTE THAT CUSTOMER REPAIR OR MODIFICATION OF THE PDI RJE V.35 CARD WILL INVALIDATE WARRANTY AND RENDER THE CARD INELIGIBLE FOR REPAIR BY HEWLETT-PACKARD COMPANY. If such repair service is performed, the replaceable parts information in Chapter 5 and the service diagram in Chapter 6 will be of assistance.

5

Replaceable Parts

This chapter contains information for ordering replaceable parts for the PDI RJE V.35 card. Table 5-1 contains a list of replaceable parts, table 5-2 contains the names and addresses of the manufacturers indexed by the code numbers in table 5-1. Chapter 6 contains a diagram showing the locations of the parts on the PDI RJE V.35 card.

Replaceable Parts

Table 5-1 contains a list of replaceable parts in reference designation order. The following information is listed for each part:

1. Reference designation of the part.
2. The Hewlett-Packard part number.
3. Part number check digit (CD).
4. Total quantity.
5. Description of the part.
6. A five-digit manufacturer's code number of a typical manufacturer of the part. Refer to table 5-2 for a cross-reference of the manufacturers.

Ordering Information

To order replacement parts or to obtain information on parts, address the order or inquiry to the nearest Hewlett-Packard Sales and Service Office (Sales and Service Offices are listed at the back of this manual).

To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number (with the check digit), and indicate the quantity required. The check digit will ensure accurate and timely processing of your order.

To order a part that is not listed in the replaceable parts table, specify the following information:

1. Identification of the kit containing the part (refer to the product identification information supplied in Chapter 1).
2. Description and function of the part.
3. Quantity required.

Table 5-1. HP 98641A Option 001 Replaceable Parts

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
	98641-66510	1	1	PC BOARD ASSEMBLY	28480	98641-66510
C1	0160-6500	7	22	CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-6500
C2	0160-6500	7		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-6500
C3	0180-0197	8	2	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
C4	0160-6500	7		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-6500
C5	0160-6500	7		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-6500
C6	0160-6500	7		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-6500
C7	0160-6500	7		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-6500
C8	0180-1746	5	1	CAPACITOR-FXD 15UF+-10% 20VDC CER	56289	150D156X902082
C9	0180-0393	6	1	CAPACITOR-FXD 39UF +-10% 10VDC TA	56289	150D396X901082
C10	0160-6500	7		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-6500
C12	0160-6500	7		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-6500
C13	0160-6500	7		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-6500
C14	0160-6500	7		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-6500
C15	0160-4807	3	1	CAPACITOR-FXD 33PF +-5% 100 VDC CER 0+-30	28480	0160-4870
C16	0160-6500	7		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-6500
C17	0160-6500	7		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-6500
C18	0160-6500	7		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-6500
C19	0160-6500	7		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-6500
C20	0160-6500	7		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-6500
C21	0160-6500	7		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-6500
C22	0160-6500	7		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-6500
C23	0160-6500	7		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-6500
C24	0160-6500	7		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-6500
C25	0160-6500	7		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-6500
C26	0160-6500	7		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-6500
C27	0160-6500	7		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-6500
C40	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
CR1	1901-0025	2	1	DIODE-GEN PRP 100V 200MA DO-7	28480	1901-0025
CR2	1902-3002	3	2	DIODE-ZRN 2.37V 5% DO-7 PD=.4W TC=-.074%	28480	1902-3002
CR3	1901-0518	8	2	DIODE-SM SIG SCHOTTKY	28480	1901-0518
CR4	1901-0518	8		DIODE-SM SIG SCHOTTKY	28480	1901-0518
CR10	1902-0049	2	1	DIODE-ZENER 6.19V	28480	1902-0049
CR11	1902-3002	3		DIODE-ZRN 2.37V 5% DO-7 PD=.4W TC=-.074%	28480	1902-3002
F1	2110-0712	8	3	FUSE 4A 125V SUBMINIATURE	28480	2110-0712
F2	2110-0712	8		FUSE 4A 125V SUBMINIATURE	28480	2110-0712
F3	2110-0712	8		FUSE 4A 125V SUBMINIATURE	28480	2110-0712
Q1	1854-0019	3	1	TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
Q2	1853-0015	7	1	TRANSISTOR PNP SI PD=200MW FT=500MHZ	28480	1853-0015
Q3	1854-0215	1	3	TRANSISTOR NPN, 2N3904	28480	1854-0215
Q4	1854-0215	1		TRANSISTOR NPN, 2N3904	28480	1854-0215
Q5	1854-0215	1		TRANSISTOR NPN, 2N3904	28480	1854-0215
R1	0683-1055	5	1	RESISTOR 1M 5% .25W CF TC=0-800	28480	0683-1055
R5	0698-0082	7	4	RESISTOR 464 1% .125W F TC=0+-100	24546	CT4-1/8-TO-4640-F
R6	0757-0405	4	1	RESISTOR 162 1% .125W F TC=0+-100	24546	C4-1/8-TO-1628-F
R7	0698-0082	7		RESISTOR 464 1% .125W F TX=0+-100	24546	CT4-1/8-TO-4640-F
R8	0698-0082	7		RESISTOR 464 1% .125W F TX=0+-100	24546	CT4-1/8-TO-4640-F
R9	0698-0082	7		RESISTOR 464 1% .125W F TX=0+-100	24546	CT4-1/8-TO-4640-F
R10	0757-0346	2	2	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-TO-10R0-F
R11	0757-0346	2	2	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-TO-10R0-F
R13	0698-0083	8	1	RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1961-F
R14	1810-0561	8	1	NETWORK-RES 16-DIP6.8K OHM X 15	28480	1810-0561
R15	1810-0517	4	1	NETWORK-RES 10 SIP6.0K OHM X 9	28480	1810-0517
SW1	3101-2747	5	2	SWITCH ASSEMBLY, 8-POSITION DIP	28480	3101-2747
SW2	3101-2747	5		SWITCH ASSEMBLY, 8-POSITION DIP	28480	3101-2747
U1	1820-3778	0	1	IC DRVR TTL COMM EIA RS-423 DUAL	02237	9636ATC
U4	1820-1201	6	2	IC GATE TTL 1.5 AND QUAD 2-INP	01295	SN74LS08N
U5	1820-1491	6	1	IC BFR TTL LS NONOINV HEX 1-INP	01295	SN74LS367AN
U6	1820-1997	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRI-IN	01295	SN74LS374N
U7	1826-0175	3	2	IC COMPARATOR	02237	LM319N
U8	1820-2703	5	1	IC DRVR TTL DIFF LINE QUAD	28480	1820-2703

Table 5-1. HP 98641A Replaceable Parts

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
	98641-66501	5	1	PC BOARD ASSEMBLY	28480	98641-66501
C1	0160-3847	9	22	CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C2	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C3	0180-0197	8	1	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
C4	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C5	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C6	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C7	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C8	0180-1746	5	1	CAPACITOR-FXD 15UF+-10% 20VDC CER	56289	150D156X902082
C9	0180-0393	6	1	CAPACITOR-RXD 39UF +-10% 10VDC TA	56289	150D396X901082
C10	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C12	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C13	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C14	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C15	0160-4807	3	1	CAPACITOR-FXD 33PF +-5% 100 VDC CER 0+-30	28480	0160-4870
C16	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C17	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C18	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C19	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C20	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C21	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C22	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C23	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C24	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C25	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C26	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C27	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
CR1	1901-0025	2	1	DIODE-GEN PRP 100V 200MA DO-7	28480	1901-0025
CR2	1902-3002	3	1	DIODE-ZRN 2.37V 5% DO-7 PD=.4W TC=-.074%	28480	1902-3002
CR3	1901-0518	8	2	DIODE-SM SIG SCHOTTKY	28480	1901-0158
CR4	1901-0158	8		DIODE-SM SIG SCHOTTKY	28480	1901-0518
F1	2110-0592	4	1	FUSE 4A 125V NTD .281X.093	28480	2110-0592
F2	2110-0592	8	1	FUSE 4A 125V NTD .281X.093	28480	2110-0592
F3	2110-0592	4		FUSE 4A 125V NTD .281X.093	28480	2110-4832
Q1	1854-0019	3	1	TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
Q2	1853-0015	7	1	TRANSISTOR PNP SI PD=200MW FT=500MHZ	28480	1853-0015
R1	0683-1055	5	3	RESISTOR 1M 5% .25W CF TC=0-800	28480	0683-1055
R2	0683-1055	5		RESISTOR 1M 5% .25V CF TC=0-800	24840	0683-1055
R3	0757-0449	6	1	RESISTOR 20K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-2002-F
R4	0683-1055	5		RESISTOR 1M 5% .25V CF TC=0-800	24840	0683-1055
R5	0698-0082	7	4	RESISTOR 464 1% .125W F TC=0+-100	24546	CT4-1/8-T0-4640-F
R6	0757-0405	4	1	RESISTOR 162 1% .125W F TC=0+-100	24546	C4-1/8-T0-1628-F
R7	0698-0082	7		RESISTOR 464 1% .125W F TX=0+-100	24546	CT4-1/8-T0-4640-F
R8	0698-0082	7		RESISTOR 464 1% .125W F TX=0+-100	24546	CT4-1/8-T0-4640-F
R9	0698-0082	7		RESISTOR 464 1% .125W F TX=0+-100	24546	CT4-1/8-T0-4640-F
R10	0757-0346	2	2	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R11	0757-0346	2	2	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R12	0698-0083	8	2	RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1961-F
R13	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1961-F
R14	1810-0561	8	1	NETWORK-RES 16-DIP6.8K OHM X 15	28480	1810-0561
R15	1810-0517	4	2	NETWORK-RES 10 SIP6.0K OHM X 9	28480	1810-0517
R16	1810-0517	4	2	NETWORK-RES 10 SIP6.0K OHM X 9	28480	1810-0517
R17	1810-0162	5	1	NETWORK-RES 14 DIP4.7K OHM X 13	11236	760-1-R4.7K
SW1	3101-2510	0	2	SWITCH ASSEMBLY-ROCKER20.0000-MHZ 0.01%	28480	3101-2510
SW2	3101-2510	0		SWITCH ASSEMBLY-ROCKER20.0000-MHZ 0.01%	28480	3101-2510
U1	1820-3778	0	4	IC DRVR TTL COMM EIA RS-423 DUAL	02237	9636ATC
U2	1820-3778	0		IC DRVR TTL COMM EIA RS-423 DUAL	02237	9636ATC
U3	1820-3778	0		IC DRVR TTL COMM EIA RS-423 DUAL	02237	9636ATC
U4	1820-1201	6	1	IC GATE TTL 1.5 AND QUAD 2-INP	01295	SN74LS08N
U5	1820-1491	6	1	IC BFR TTL LS NONOINV HEX 1-INP	01295	SN74LS367AN
U6	1820-1997	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRI-IN	01295	SN74LS374N
U7	1820-3778	0		IC DRVR TTL COMM EIA RS-423 DUAL	02237	9636ATC
U8	1820-2703	5	1	IC DRVR TTL DIFF LINE QUAD	28480	1820-2703

Table 5-1. HP 98641A Replaceable Parts

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
U9	1820-2594	7	2	IC RCVR TTL LS LINE RCVR QUAD 2 INP	28480	1820-2594
U10	1820-2594	2	2	IC RCVR TTL LS LINE RCVR QUAD 2 INP	28480	1820-2594
U11	1820-1244	7	1	IC MUXR/DATA-SFL TTL LS 4-TO-1-1 INF DUAL	01295	SN741LS153N
U12	1820-2301	9	1	IC-Z80A CTC	28480	1820-2301
U13	1820-1112	8	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U14	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U15	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U16	1820-2657	8	2	IC GATE TTL ALS OR QUAD 2-INP	01295	SN74ALS32N
U17	1820-0693	8	2	IC FF TTL S D-TYPE POS-EDGE TRIG	01295	SN74S74N
U18	1813-0225	7	1	CRYSTAL-CLOCK-OSCILLATOR	28480	1813-0225
U19	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE TRIG	01295	SN74S74N
U20	1820-1438	1	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U21	1820-1245	8	2	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS155N
U22	1820-1245	8		IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS155N
U23	1820-1440	5	1	IC LCH TTL LS QUAD	01295	SN74LS279N
U24	1820-2739	7	1	IC GATE TTL ALS NOR QUAD 2-INP	01295	SN74ALS02N
U25	1818-3198	7	1	IC RAM	S4013	HM6264P-15
U27	1820-2300	8	1	IC-Z80A SIO/2	28480	1820-2300
U28	1820-2298	3	1	IC-Z80A CPU	28480	1820-2298
	1200-0817	4	1	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0817
U29	98641-81003	5	1	EPROM	28480	98641-81003
	1200-0861	5	1	SOCKET-IC 28-COUNT DIP-SOLDER	28480	1200-0861
U30	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U31	1820-1281	2	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS139N
U32	1820-1428	9	1	IC MUXR/DATA-SFL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS159N
U33	1820-1438	1		IC MUXR/DATA-SFL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U34	1820-1427	8	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS156N
U35	1820-1568	8	1	IC BFR TTL LS BUS QUAD	01295	SN74LS125AN
U36	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
U37	1820-2657	8		IC GATE TTL ALS OR QUAD 2-INP	01295	SN74LS32N
U38	1820-1905	7	1	IC GATE TTL LS NOR DUAL 5-INP	07263	74LS260PC
U39	1820-1444	9	4	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS298N
U40	1820-1444	9		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS298N
U41	1820-1444	9		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS298N
U42	1820-1444	9		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS298N
U43	1820-2740	0	1	IC COMPTR TTL LS MAGID 2-INP 8-BIT	01295	SN74LS688N
U44	1820-2206	3	2	IC MISC TTL LS	01295	SN74LS640N
U45	1820-2206	3	2	IC MISC TTL LS	01295	SN74LS640N
W1	1258-0124	7	3	PIN-PROGRAMMING JUMPER .30 CONTACT	91506	8136-475G1
	1200-0455	6	1	SOCKET-IC 8-CONT DIP-SLDR	28480	1200-0455
W2	1258-0124	7		PIN PROGRAMMING JUMPER .30 CONTACT	91506	8136-475G1
W3	1258-0124	7		PIN PROGRAMMING JUMPER .30 CONTACT	91506	8136-475G1
				MISCELLANEOUS		
	0380-1324	9	2	STANDOFF-THD	28490	0380-1324
	0515-0145	7	2	SCREW-MACH M3 X 0.5 8MM-LG 90-DEG-FLH-HD	00000	ORDER BY DESCRIPTION
	1251-2248	6	2	LOCK SPRING-MICRO RBN CONN	28480	1251-2248
	1251-7119	0	2	END DISC-LATCH	28480	1251-7119
	1251-8949	2	1	CONNECTOR-50 POST RING	28480	1251-8949
	2380-0001	9	2	SCREW MACH 6-32 .25-IN-LG FTL-HD SLT	00000	ORDER BY DESCRIPTION
	98641-00001	3	1	I/O COVER	28480	98641-00001
	5061-4215	2	1	CABLE DIE INTERFACE (FEMALE CONNECTOR)	28480	5061-4215
	7121-1957	3	1	LABEL SELECT CODE	28480	7121-1957
	98641-90001	8	1	INSTALLATION MANUAL	28480	98641-90001

Table 5-2. Manufacturer's Code List

Mfr Code	Manufacturer Name	Address		Zip Code
01121	ALLEN-BRADLEY CO.	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND COMPNT DIV	DALLAS	TX	75222
02237	FAIRCHILD CORPORATION	MOUNTAIN VIEW	CA	94042
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
11236	CTS OF BERNE INC.	BERNE	IN	46711
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
91506	AUGAT INC	ATTLEBORO	MA	02703
S4013	HITACHI	JAPAN		TOYKO

6

Service Diagrams

This chapter contains a parts location diagram and a schematic logic diagram for the PDI RJE V.35 card.

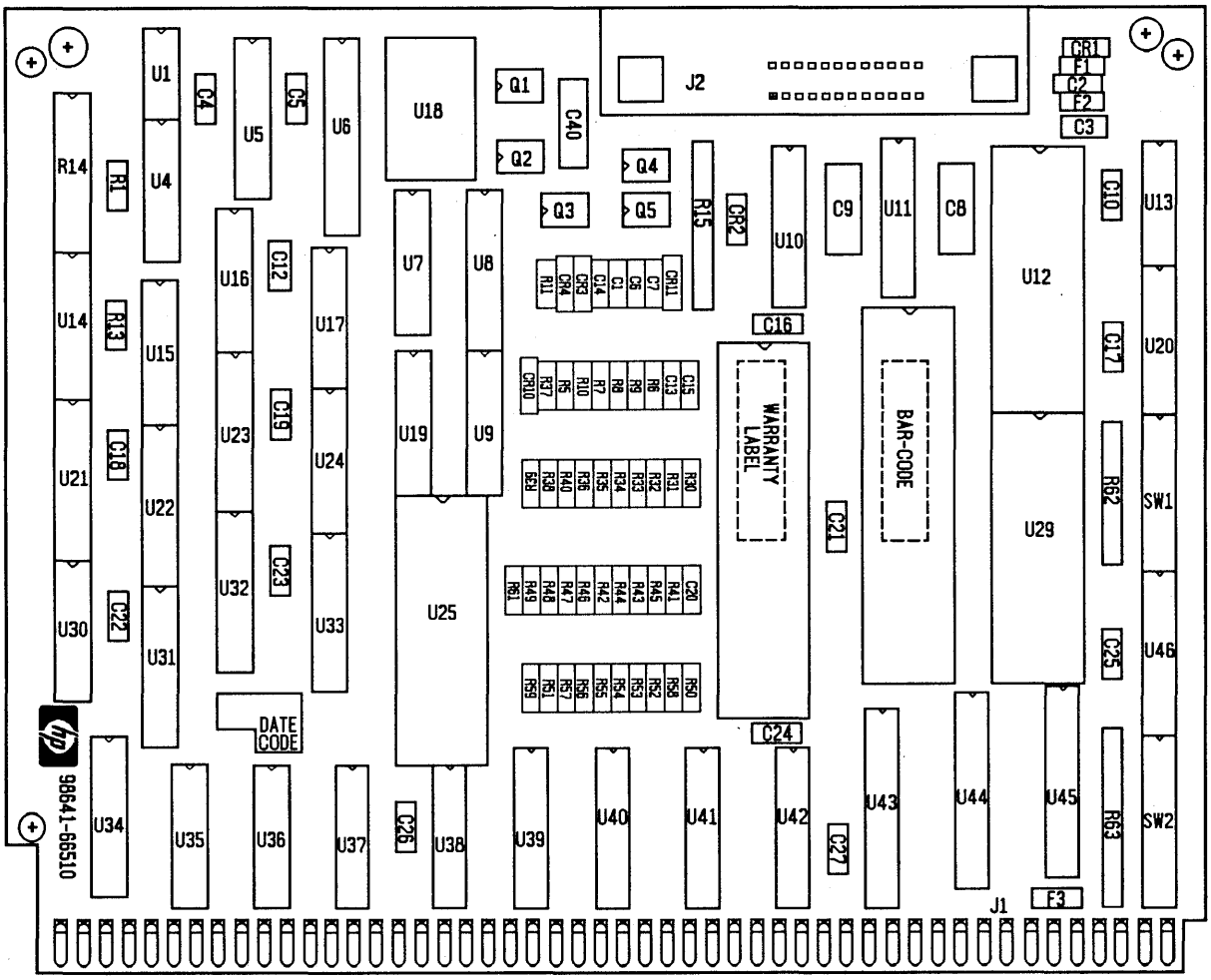


Figure 6-1. Parts Location Diagram

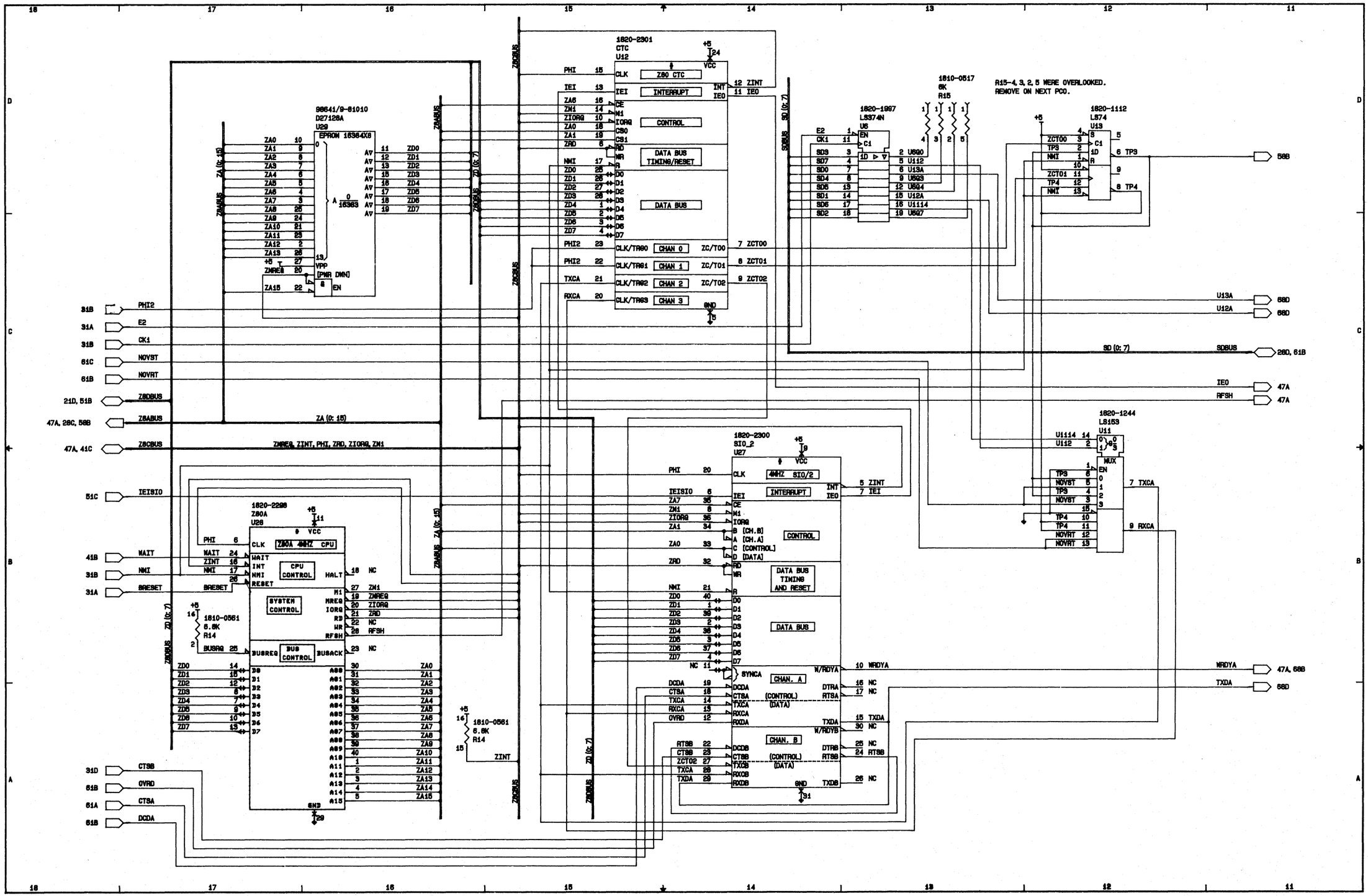
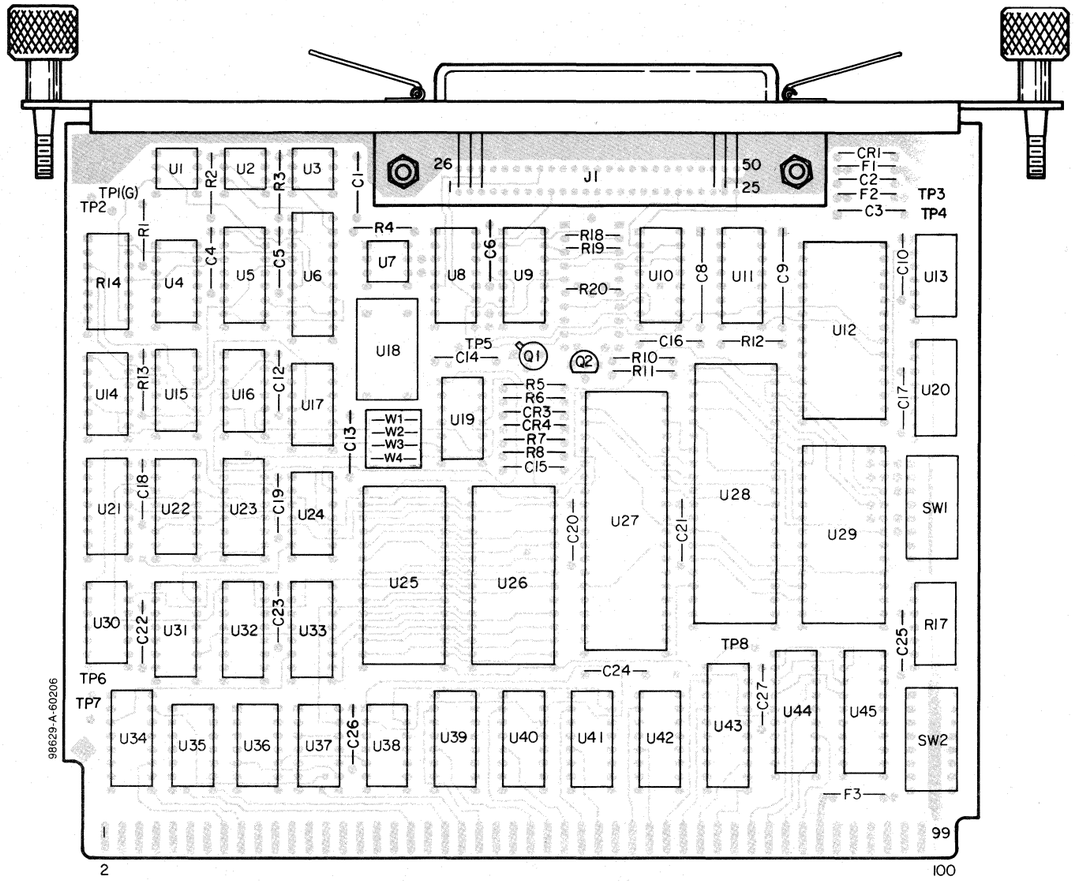


Figure 6-2. Schematic Diagram (Sheet 1 of 6)



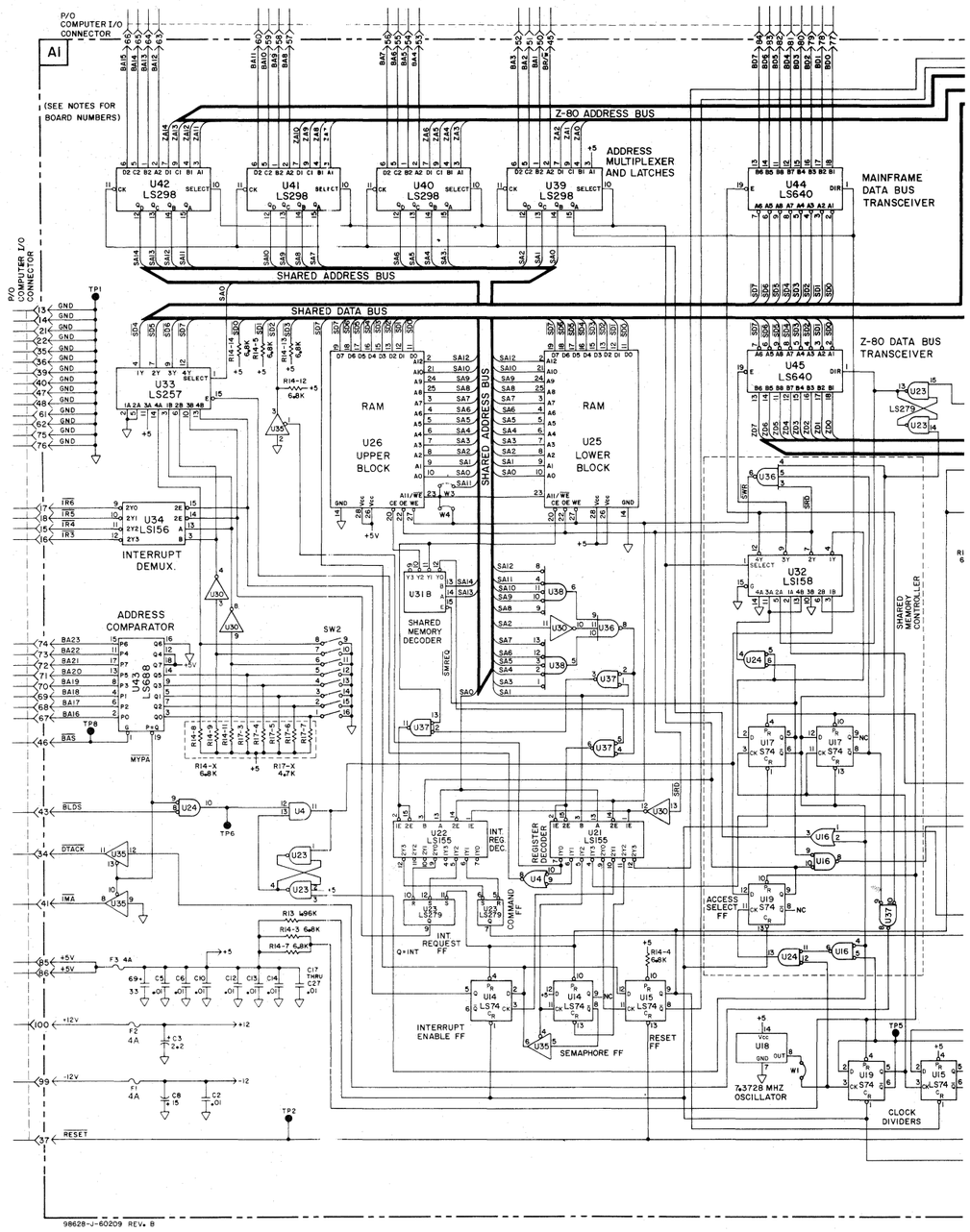
COMPONENT SIDE
A1

HP Part No. 98628-66503, 98629-66501, 98691-66501 } Rev B

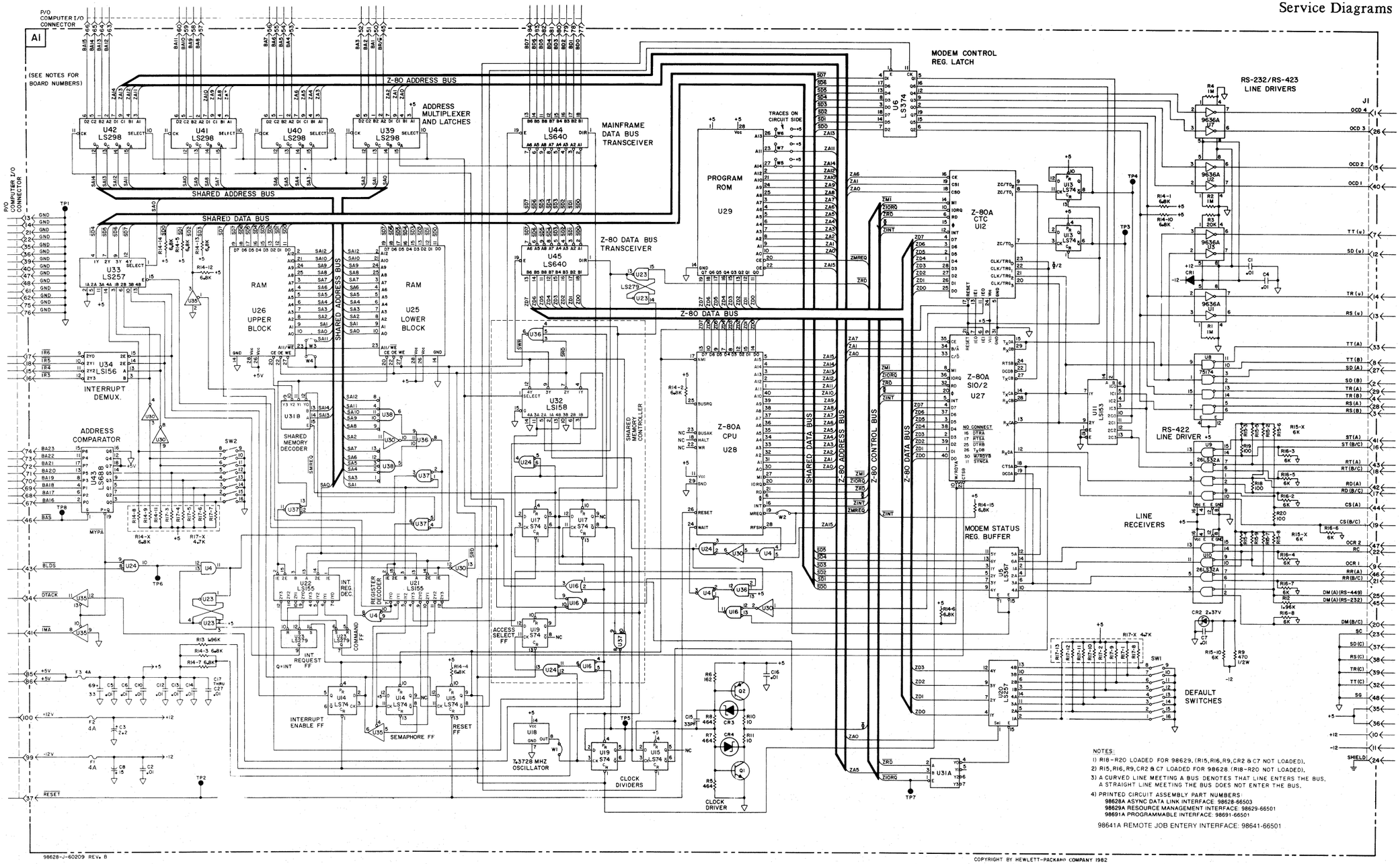
98641-66501 Rev B

SCHEMATIC NOTES

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX WITH ASSEMBLY OR SUB-ASSEMBLY
   DESIGNATION(S) OR BOTH FOR COMPLETE DESIGNATION.
2. COMPONENT VALUES ARE SHOWN AS FOLLOWS UNLESS OTHERWISE NOTED.
   RESISTANCE IN OHMS
   CAPACITANCE IN MICROFARADS
3. A CURVED LINE MEETING A BUS DENOTES THAT LINE ENTERS THE BUS, A STRAIGHT LINE MEETING THE BUS DENOTES THAT LINE DOES NOT ENTER THE BUS.
4. R18-R20 LOADED FOR 98629. R15, R16, R9, CR2, & C7 NOT LOADED.
5. R15, R16, R9, CR2, & C7 LOADED FOR 98628. R18-R20 NOT LOADED.
6. PRINTED CIRCUIT ASSEMBLY PART NUMBER:
   98628A ASYNC/DATA LINK INTERFACE: 98628-66503
   98629A RESOURCE MANAGEMENT INTERFACE: 98629-66501
   98691A PROGRAMMABLE INTERFACE: 98691-66501
   98641A REMOTE JOB ENTRY INTERFACE: 98641-66501
7. NOTE TO W5,W6,W7:
   W5,6,AND 7 ARE PROVIDED FOR USE WITH EPROMS ON THE 98691. TO CHANGE INPUTS TO +5V, THE TRACES TO ZA11, ZA13, AND ZA14 MUST BE CUT BEFORE INSTALLING JUMPERS TO +5V PADS. TO RESTORE NORMAL CONFIGURATION, REMOVE JUMPERS TO +5V AND INSTALL THEM IN THEIR ZAxx CONNECTED POSITIONS.



8. NOTE TO W3, W4, W5:
   W3 AND W4 ARE PROVIDED FOR RAM CONFIGURATION AND W5 IS PROVIDED FOR USE WITH EPROM ON THE 98641. FOR THE 98641 RAM, JUMPER W4 IS REMOVED AND JUMPER W3 IS INSTALLED. FOR THE 98641 EPROM, TRACE W5, BETWEEN A14 AND ZA14, IS CUT AND A14 JUMPERED TO +5U.



8. NOTE TO W3, W4, W5:
W3 AND W4 ARE PROVIDED FOR RAM CONFIGURATION AND W5 IS PROVIDED FOR USE WITH EPROM ON THE 98641. FOR THE 98641 RAM, JUMPER W4 IS REMOVED AND JUMPER W3 IS INSTALLED. FOR THE 98641 EPROM, TRACE W5, BETWEEN A14 AND ZA14, IS CUT AND A14 JUMPERED TO +5U.

Figure 6-1. PDI RJE Service Diagrams
Update 1 (August 1986)
6-3/6-4

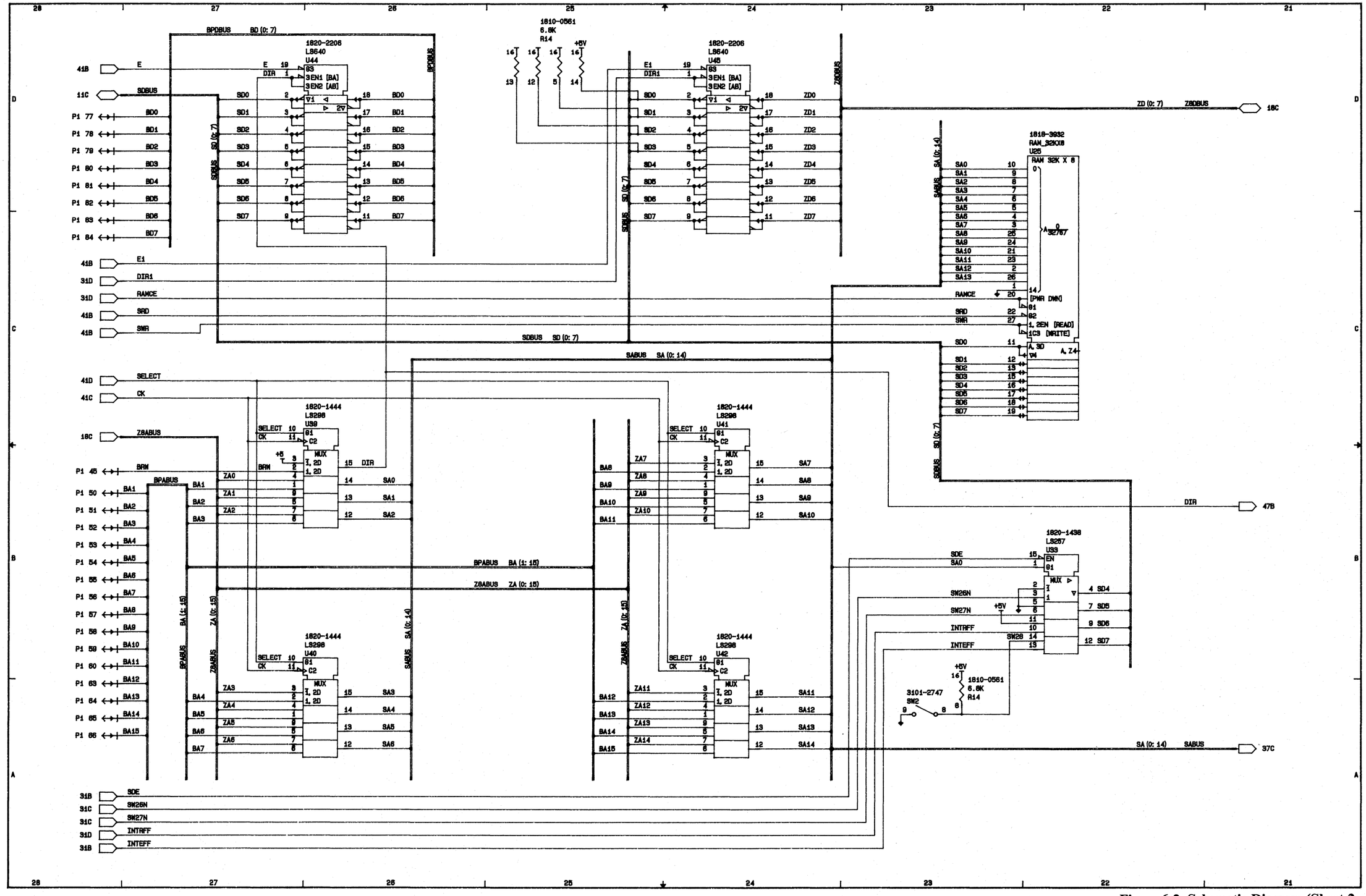


Figure 6-2. Schematic Diagram (Sheet 2 of 6)

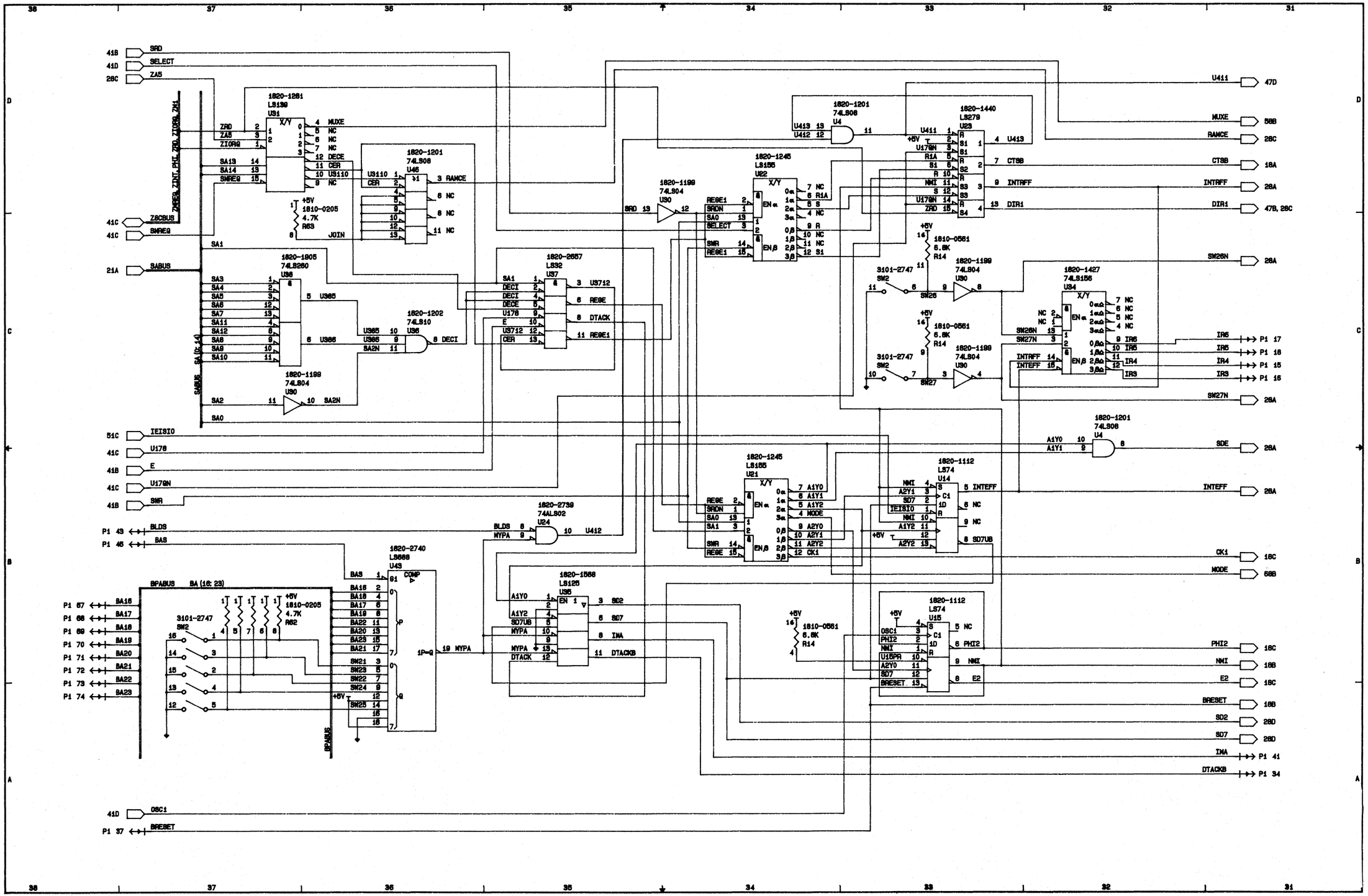


Figure 6-2. Schematic Diagram (Sheet 3 of 6)

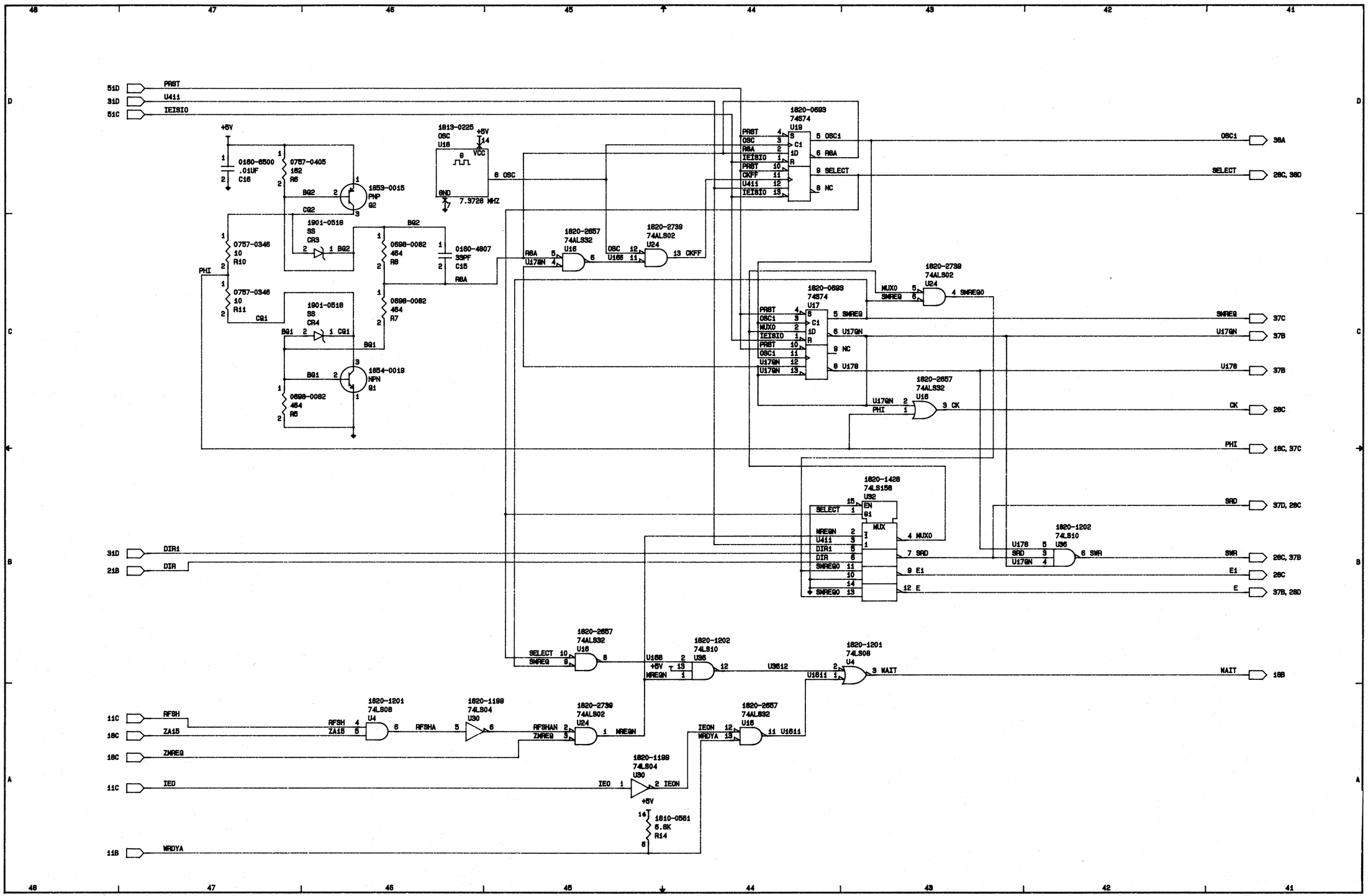


Figure 6-2. Schematic Diagram (Sheet 4 of 6)

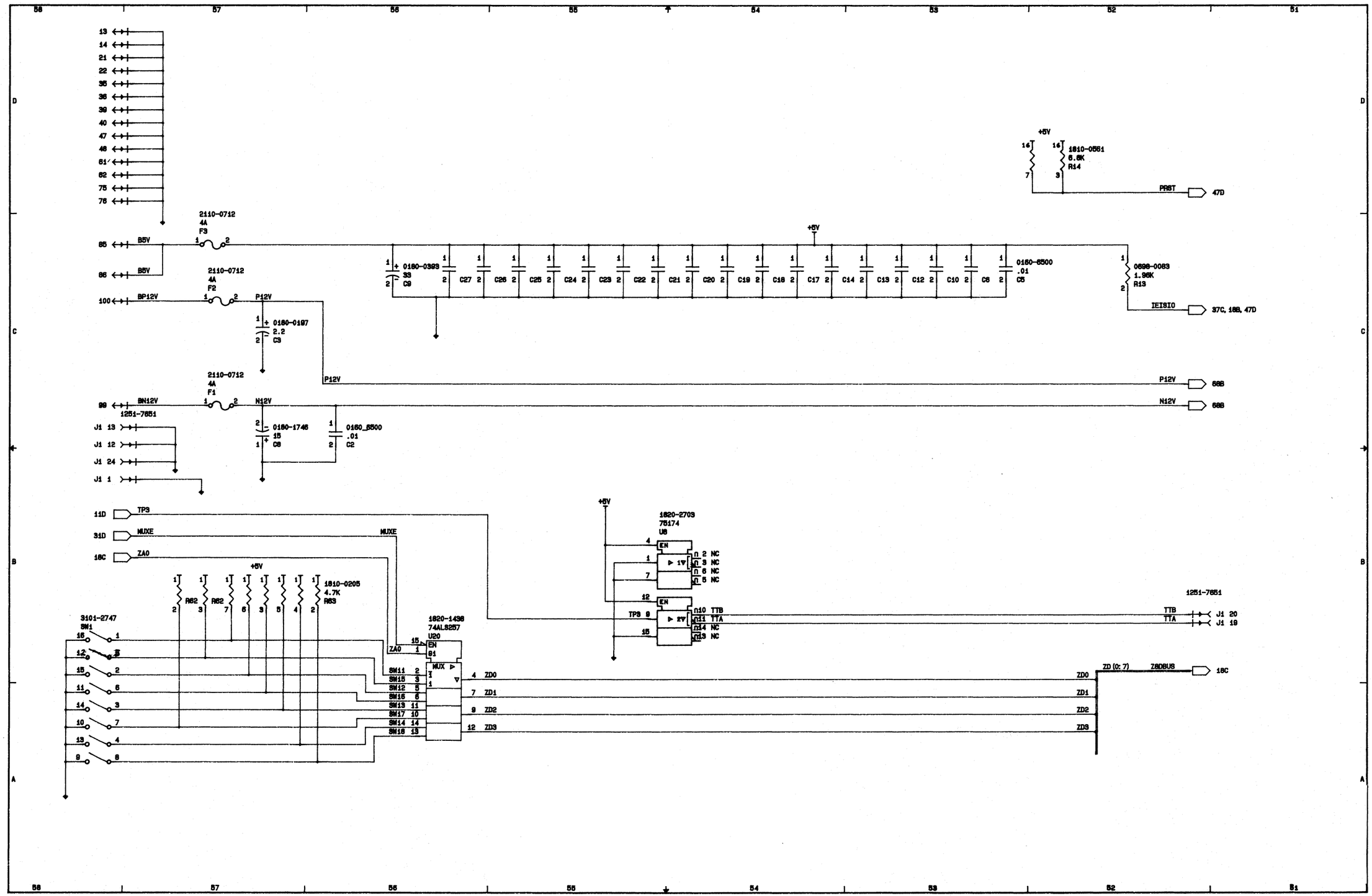


Figure 6-2. Schematic Diagram (Sheet 5 of 6)

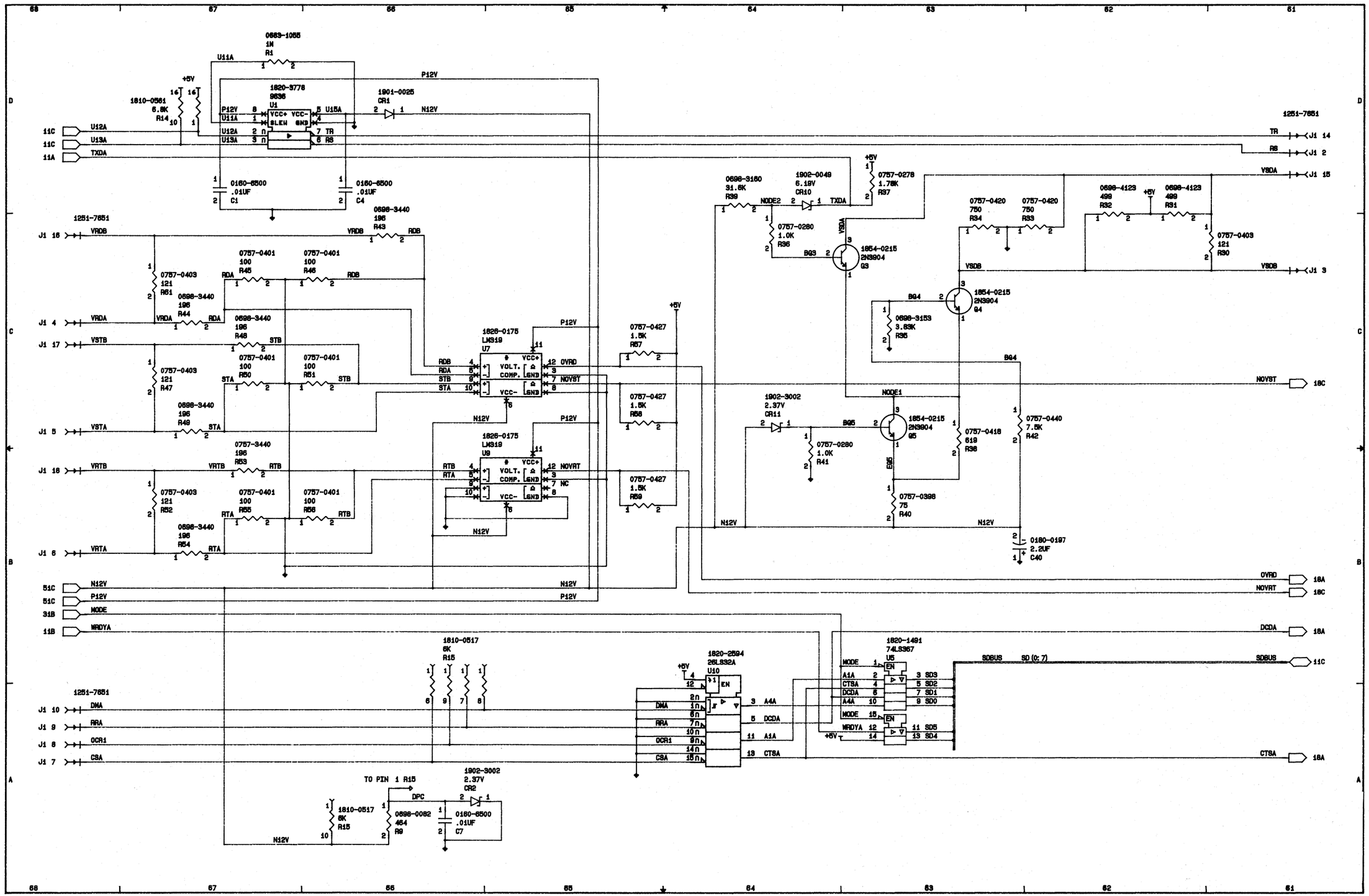


Figure 6-2. Schematic Diagram (Sheet 6 of 6)

Chapter 7
Product History

This chapter lists the changes that have been made to the HP98641A PDI RJE.

Date Code	Remarks
B-2428	Original board.
B-2528	Line drivers (U1, U2, U3, and U7) changed from 1820-2117 to 1820-3778.
B-2627	EPROM changed from 98641-81001 to 98641-81003.

A

V.35 Cable Information

This appendix shows a drawing of the V.35 cable (Figure A-1) with the connector pins labeled for both connectors. Also, table A-1 shows the two connector pin labels, the names of the signals on each of the pins, and the function of those signals.

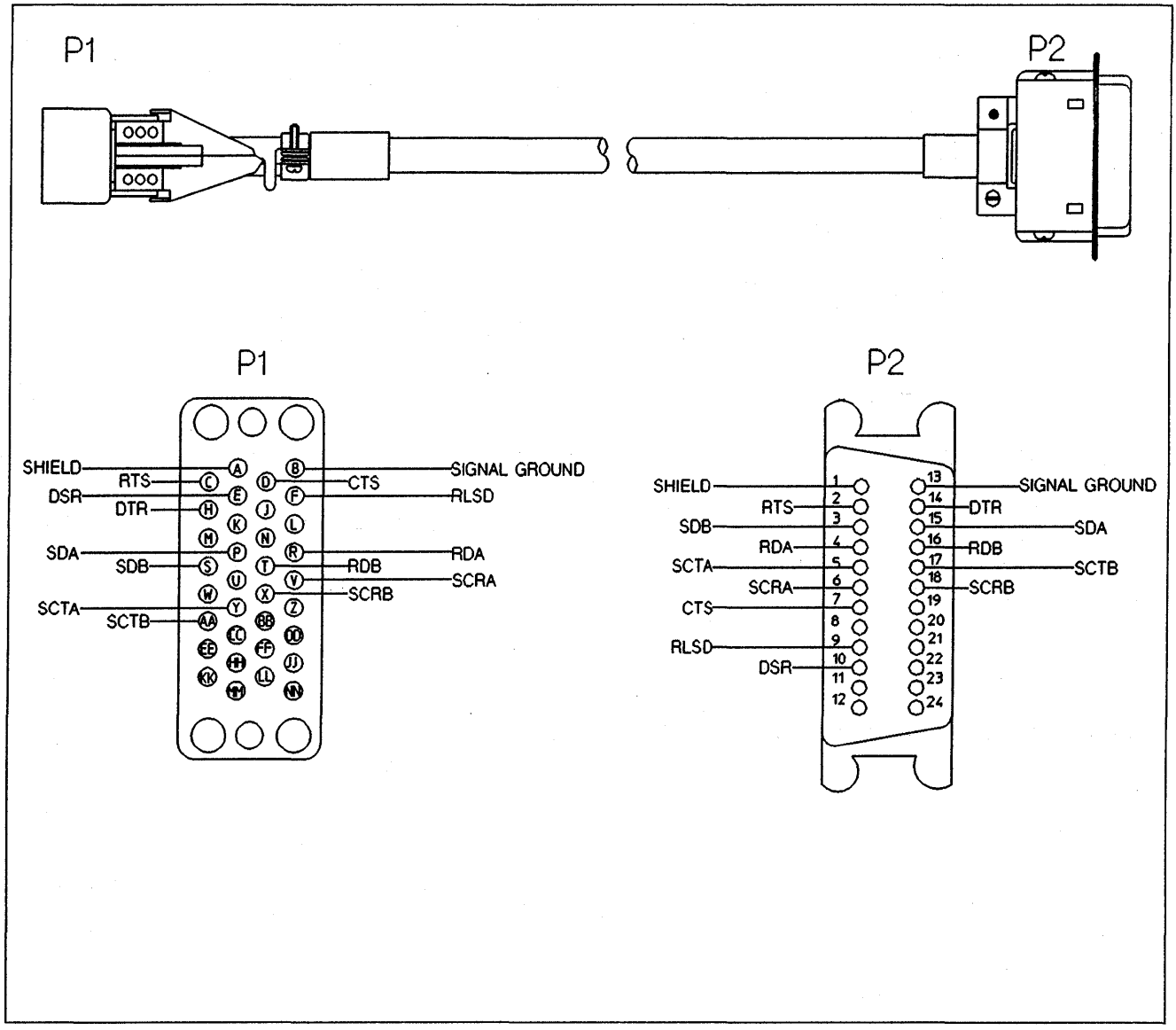


Figure A-1. V.35 Cable

Table A-1. V.35 Cable Pin Descriptions

P1 PIN	P2 PIN	NAME	FUNCTION
A	1	-----	Shield Ground
B	13	-----	Signal Ground
C	2	RTS	Request To Send
D	7	CTS	Clear To Send
E	10	DSR	Data Set Ready
F	9	RLSD	Received Line Signal Detect
H	14	DTR	Data Terminal Ready
P	15	SDA	Send Data (Signal A)
R	4	RDA	Received Data (Signal A)
S	3	SDB	Send Data (Signal B)
T	16	RDB	Received Data (Signal B)
V	6	SCRA	Serial Clock Receive (Signal A)
X	18	SCRB	Serial Clock Receive (Signal B)
Y	5	SCTA	Serial Clock Transmit (Signal A)
AA	17	SCTB	Serial Clock Transmit (Signal B)

Unused Pins on P1 - J, K, L, M, N, U, W, Z, BB, CC, DD, EE, FF, HH, JJ, KK, LL, MM, NN

Unused Pins on P2 - 8, 11, 12, 19, 20, 21, 22, 23, 24

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